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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,166	09/24/2003	Toshio Kimura	1035-473	4031

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,166	KIMURA ET AL.	
	Examiner	Art Unit	
	Quang D. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,534,879 to Terui.

Regarding claim 1, Terui (figures 5A-B) teaches a semiconductor device, comprising:

a plurality of spaced apart through electrodes (electrodes [285, 285, 183]) with equal cross-sectional areas in a semiconductor chip (60) linking a front surface (upper surface [60]) to a back surface (lower surface [60]) thereof;

a first number of adjacent ones of the plurality of through electrodes (power electrodes [285]) being electrically connected to one another to form a power-supply through electrode and in communication with a power supply (power terminal [85]), a second number of adjacent ones of the plurality of through hole electrodes (ground electrodes [287]) being electrically connected to one another to form a grounding through-electrode and in communication with ground (ground terminal [87]), and wherein only one of the plurality of through electrodes (signal electrode [183]) is used to form a particular signal-routing through electrode; and

wherein at least one of the first number (power electrode [285]) and the second number (ground electrode [287]) is two (285, 287), so that at least one of the power-supply through electrode (power electrode [285]) and the grounding through electrode (ground electrode [287]) is made up of at least two adjacent ones of the through electrodes (285, 287) which are electrically connected to one another, whereas the signal-routing electrode is made up of only one of the through electrodes (a signal electrode [183]).

Regarding claim 2, Terui teaches at least one type of the through electrodes (285) is contact through electrodes (287) electrically connected to that semiconductor chip (60).

Regarding claim 3, Terui teaches at least one type of the through electrodes (40) is non-contact through electrodes not electrically connected to that semiconductor chip (60).

Regarding claim 4, Terui teaches both of the first number (285) and the second number (287) is two (285, 287), so that each of the power-supply through electrode (power electrode [285]) and the grounding through electrode (ground electrode [287]) is made up of at least two adjacent ones of the through electrodes (285, 287) which are electrically connected to one another, whereas the signal-routing electrode is made up of only one of the through electrodes (a signal electrode [183]).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,534,879 to Terui in view of Japan Patent No. 08-213427 to Naoyuki.

Regarding claim 5, Terui differs from the claimed invention by not showing multiple stacked semiconductor chips. However, Naoyuki (figures 1-4) teaches the stacked chips (stacked chips [15, 16D, 16E]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Naoyuki into the device taught by Terui in order to increase the chip density and the number of connection in the device.

Regarding claim 6, Terui (figures 5A-B) teaches a chip-stack semiconductor device, comprising:

the semiconductor chip (60) including a number of through electrodes (electrodes [285, 285, 183]) with equal cross-sectional areas therein linking a front surface (an upper surface [285, 287, 183]) to a back surface (a lower surface [285, 287, 183]) thereof, and at least one type of the through electrodes (electrodes [285, 287, 183]) is contact through electrodes electrically connected to that semiconductor chip (60); and

wherein at least one of a power supply through-electrode (power electrode [285]) connected to a power supply (power terminal [85]) and a grounding through-electrode (ground electrode [287]) connected to ground (power terminal [85]) is made up of at least two adjacent ones of the through electrodes (285, 287) which are electrically connected to one another, whereas a signal electrode is made up of only one of the through electrodes (a signal electrode [183]).

Terui differs from the claimed invention by not showing a plurality of stacked semiconductor chips. However, Naoyuki (figures 1-4) teaches the stacked chips (stacked chips

[15, 16D, 16E]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Naoyuki into the device taught by Terui in order to increase the chip density and the number of connection in the device.

Regarding claim 7, Terui (figures 5A-B) teaches a chip-stack semiconductor device, comprising:

each of the semiconductor chip (60) including a number of through electrodes (electrodes [285, 285, 183]) with equal cross-sectional areas therein linking a front surface (an upper surface [285, 287, 183]) to a back surface (a lower surface [285, 287, 183]) thereof, and at least one type of the through electrodes (40) is non-contact through electrodes not electrically connected to that semiconductor chip (60); and

wherein at least one of a power supply through-electrode (power electrode [285]) connected to a power supply (power terminal [85]) and a grounding through-electrode (ground electrode [287]) connected to ground (power terminal [85]) is made up of at least two adjacent ones of the through electrodes (285, 287) which are electrically connected to one another, whereas a signal electrode is made up of only one of the through electrodes (a signal electrode [183]).

Terui differs from the claimed invention by not showing a plurality of stacked semiconductor chips. However, Naoyuki (figures 1-4) teaches the stacked chips (stacked chips [15, 16D, 16E]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Naoyuki into the device taught by Terui in order to increase the chip density and the number of connection in the device.

Regarding claim 8, Terui (figures 5A-B) teaches the semiconductor chip (60) including a number of through electrodes (electrodes [285, 287, 183]) with equal cross sectional areas therein linking a front surface (an upper surface [285, 287, 183]) to a back surface (a lower surface [285, 287, 183]) thereof, the number of the through electrodes (285, 287, 183) being determined according to a magnitude of an electric current with respect to an identical signal; and

a number of adjacent connected ones of the through electrodes (power electrodes [285] and ground electrodes [287]) which are connected to a power terminal (power terminal [85]) of that semiconductor chip is greater than a number of adjacent connected ones of the through electrodes (signal electrodes [183]) which are connected to a particular signal terminal (signal terminal [83]) thereof.

Terui differs from the claimed invention by not showing a plurality of stacked semiconductor chips. However, Naoyuki (figures 1-4) teaches the stacked chips (stacked chips [15, 16D, 16E]). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Naoyuki into the device taught by Terui in order to increase the chip density and the number of connection in the device.

Regarding claim 9, the combined device shows a number of those through electrodes which connect n+1 (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips [16D, 16E, 15]) is greater than a number of those through electrodes which connect n (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips [16A, 15]).

Regarding claim 10, the combined device shows a number of those through electrodes which connect n+1 (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips

[16D, 16E, 15]) is greater than a number of those through electrodes which connect n (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips [16A, 15]).

Regarding claim 11, the combined device shows a number of those through electrodes which connect n+1 (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips [16D, 16E, 15]) is greater than a number of those through electrodes which connect n (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips [16A, 15]).

Regarding claim 12, the combined device shows a number of those through electrodes which connect n+1 (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips [16D, 16E, 15]) is greater than a number of those through electrodes which connect n (n is more than or equal 2) adjacent semiconductor chips (Naoyuki; chips [16A, 15]).

Regarding claim 13, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased according to an interconnect line length through the multiple stacked semiconductor chips (stacked chips [15, 16D, 16E]).

Regarding claim 14, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased according to an interconnect line length through the multiple stacked semiconductor chips (Naoyuki; stacked chips [15, 16D, 16E]).

Regarding claim 15, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased according to an interconnect line length through the multiple stacked semiconductor chips (Naoyuki; stacked chips [15, 16D, 16E]).

Regarding claim 16, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased according to an interconnect line length through the multiple stacked semiconductor chips (Naoyuki; stacked chips [15, 16D, 16E]).

Regarding claim 17, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips (Naoyuki; stacked chips [15, 16D, 16E]).

Regarding claim 18, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips (Naoyuki; stacked chips [15, 16D, 16E]).

Regarding claim 19, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips (Naoyuki; stacked chips [15, 16D, 16E]).

Regarding claim 20, the combined device shows the number of the through electrodes (Naoyuki; electrodes [9]) is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips (Naoyuki; stacked chips [15, 16D, 16E]).

Response to Arguments

Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
January 18, 2005

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